METROLOGY AND MEASUREMENT SYSTEMS
Index 330930, ISSN 0860-8229
www.metrology.pg.gda.pl

# REVIEW OF SINGLE-STAGE TIME-INTERVAL MEASUREMENT MODULES IMPLEMENTED IN FPGA DEVICES

**Marek Zieliński**

*Nicolaus Copernicus University, Institute of Physics, Department of Technical and Applied Physics, Grudziądzka 5, 87-100 Toruń, Poland*
*(✉ marziel@fizyka.umk.pl, +48 56 611 3224)*

**Abstract**

High resolution Time Interval Measurement Systems [TIMS] can be applied in experimental physics, ultrasonic flow meters, distance meters, or clock period meters. In this paper the problem of single-stage, high resolution TIMS design and implementation in programmable CMOS FPGA devices is discussed. Different architectures of TIMS are compared. Moreover, main parameters of TIMS, such as resolution, double pulse resolution, nonlinearity and sensitivity to temperature fluctuation are also discussed.

Keywords: time-interval measurement, time-interval measuring module, FPGA applications.



## 1. Introduction

Many time-interval measurement methods and systems were described and discussed during the last several years in different scientific journals and conference proceedings [1-3]. From time to time, new analyses and comparison of methods and systems are necessary [4, 5]. TIMS realized as full custom CMOS chips can be optimized for their applications, however they are relatively expensive [6]. Implementation of TIMS in CMOS FPGA devices is a compromise solution. In such a way it is possible to design and implement quickly the TIMS of relatively good parameters, which is not expensive [1, 3, 7-11]. High resolution TIMS should be characterized by a resolution better than 1 ns. Fortunately, modern FPGA devices which contain transistors with a channel width less than 90 nm allow for designing TIMS with a resolution much better than 1 ns [7-11]. A high-resolution system for measurement of the life-time of excited atomic states [8], system for clock characterization [12], system for quantum cryptography experiments [13], system for ultrasonic flow-meters [14] or monitoring system of time-of-flight mass spectrometer [9, 10, 15] can be good examples of single-stage TIMS applications. Of course, it should be pointed out that systems implemented in FPGA devices need relatively much energy compared with full custom CMOS TIMS and sometimes are not suitable for battery operation.

## 2. Time-interval measurement

Most of high resolution TIMS use the measurement method shown in Fig.1 [1, 8-10]. In that method three time intervals are measured:

- $\Delta t_p$ – between the stop pulse rise transition and clock rise transition,
- $\Delta t_k$ – between the start pulse rise transition and clock rise transition,
- $\Delta t_N$ – which consists of an integer number N of standard clock periods ($\Delta t_N = NT_0$).

The result of a time-interval measurement will be given as:

$$\Delta t_m = \Delta t_N + \Delta t_p - \Delta t_k = \Delta t_p - \Delta t_k + NT_0 . \quad (1)$$

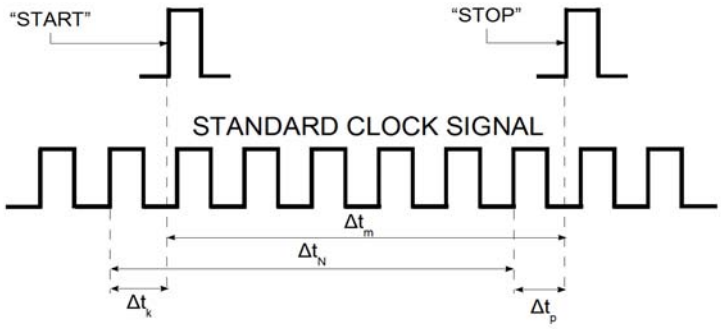


Fig. 1. Time interval measuring method.

The precision of TIMS depends in practice on the precision of interpolators which measure residual time intervals $\Delta t_p$ and $\Delta t_k$. In case of a very small time interval measurement, usually less than 1μs, the time-interval $\Delta t_m$ can be measured straight without a standard clock reference signal [1]. TIMS as a virtual instrument consists of a hardware unit, flexible software and a computer. All hardware unit elements, except the standard clock can be implemented inside a FPGA structure, as shown in Fig. 2.

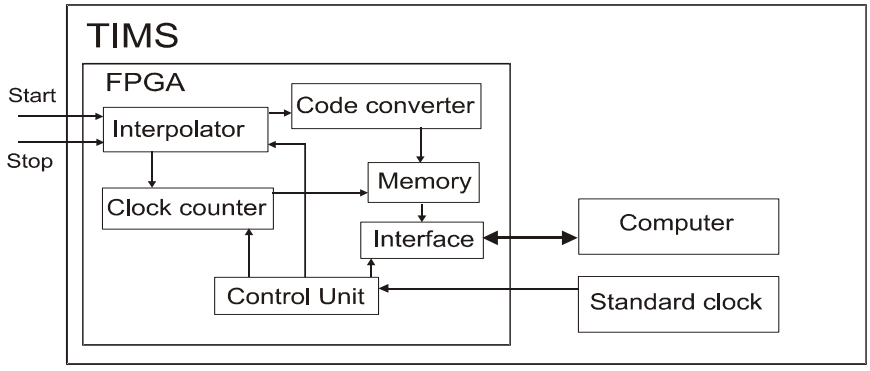


Fig. 2. Time interval measuring system.

For measurement of time-intervals greater than 1μs, TIMS which contain clock counters are usually applied. Such architectures lead directly to a more effective and flexible TIMS [8-12]. In practice the most important differences between TIMS concern the interpolator architecture and the method of interpolation. Methods of time-interval interpolation can be analog, digital or mixed [1]. The interpolator can be realized as a single- or multi-stage unit [7-11].

## 3. Time-interval measurement modules

The high-resolution time interval measurement module [TIMM] with a single-stage interpolator implemented in the FPGA structure consists of: a tapped delay line, data registers, a clock counter, code converters, a control unit and memory [8-11]. The block diagram of the TIMM is shown in Fig. 3.

In this system, time-intervals between start and stop pulses and each of clock transitions fed to the input are precisely measured using tapped delay lines and are collected in the

memory [8-11]. In order to increase the double-pulse resolution, the dead-time caused by data conversion should be strongly limited. This problem has been solved by increasing the number of code converters [10].

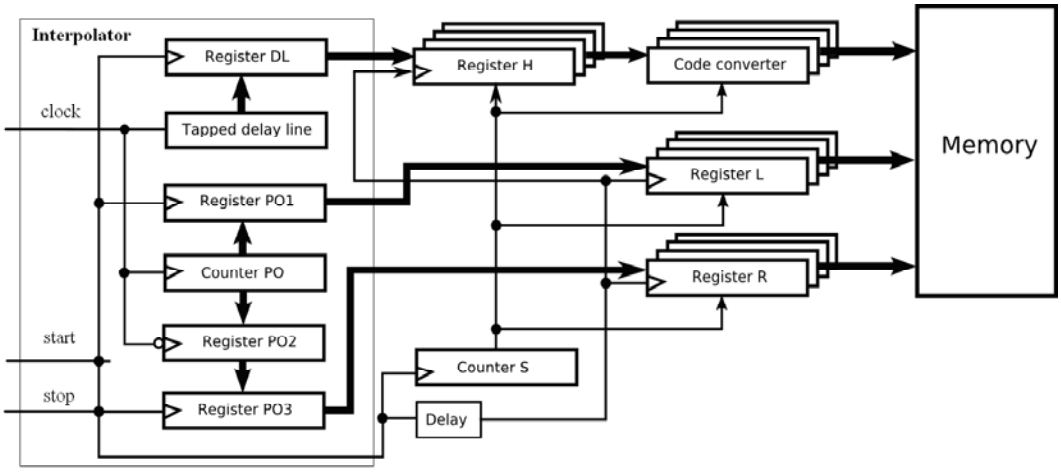


Fig. 3. Block Diagram of the TIMM implemented inside FPGA structure.

The most important part of the interpolator unit is a tapped delay line implemented also in the FPGA structure. However, all FPGA structures are generally regular and it should be pointed out that the implementation of the tapped delay line inside the FPGA structure is not easy. To solve this problem it is necessary to find many elements of the same delay which can be connected in the same way, without insertion of different delays between the delay elements [8, 9].

The first method uses Look-up-tables (LUT's) which are regularly spread in the FPGA structure, as shown in Fig. 4 [9].

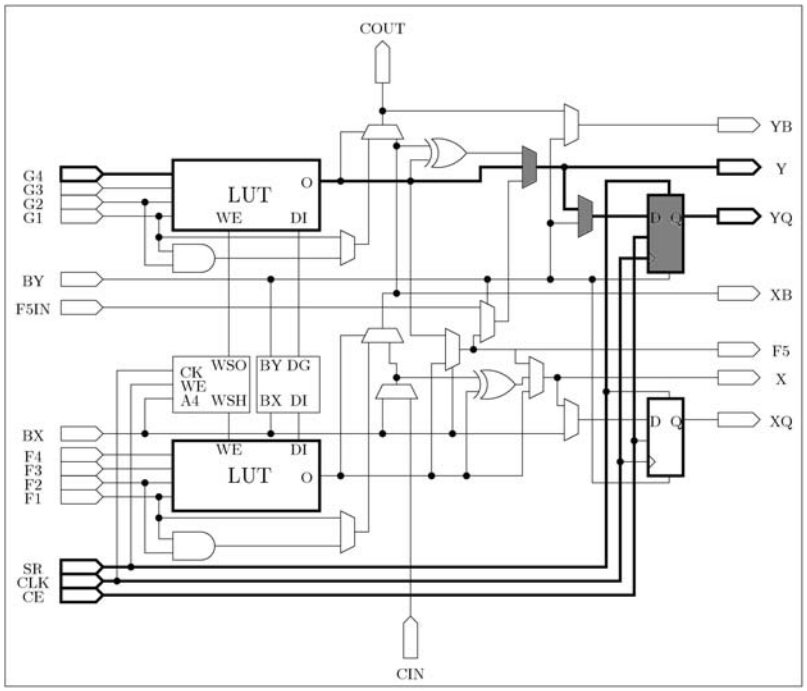


Fig. 4. Single element of a tapped delay line using LUT's.

Unfortunately, in such a case the resolution of a TIMM is strongly limited. For example, the simple tapped delay line implemented in Virtex XCV300 has a resolution of 1 ns. Fortunately, the resolution of a TIMM can be increased by using several delay lines appropriately shifted in time, as shown in Fig. 5.

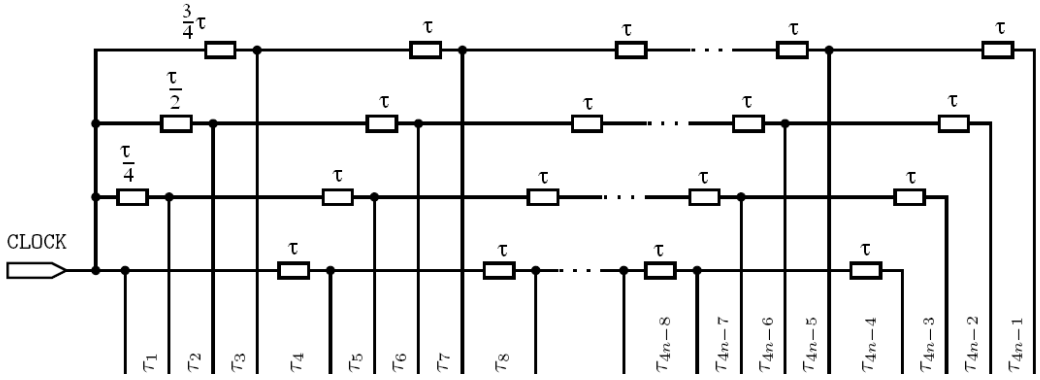


Fig. 5. Model of a multi-tapped delay line.

This method enables to design a TIMM with a resolution up to 250 ps [9]. Moreover, in this method the delay elements can be relatively easily adjusted by using tri-state buffers, as it is shown in Fig. 6 [9]. TIMMs containing tapped delay lines built using LUTs have good INL (Integral Non-Linearity) and DNL (Differential Non-Linearity) characteristics. Maximal values of INL and DNL characteristics are usually limited to 50 ps.

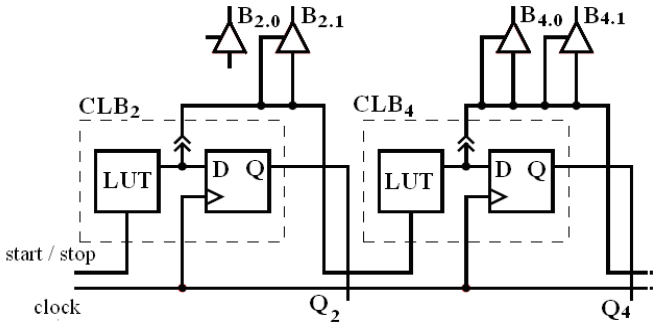


Fig. 6. Adjustment of tapped delay line by tri-state buffers.

The resolution of a TIMM can be also increased by using a differential multi-tapped delay line, as shown in Fig. 7 [1].

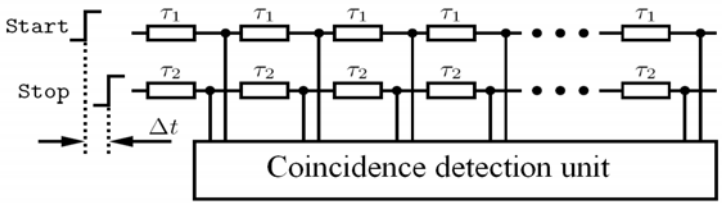


Fig. 7. Model of differential multi-tapped delay line.

The resolution of such TIMM depends on the difference between delay elements $\tau_1$ and $\tau_2$ used in the construction of delay lines. That method has a very important disadvantage. While

the delay line consists of many delay elements which have a delay time of the order of nanoseconds, the interpolation time $t_{in}$ is relatively long and can be written as:

$$t_{in} = \frac{\Delta t}{\tau_1 - \tau_2}\tau_2, \tag{2}$$

where $\Delta t$ is the measured time-interval, $\tau_1 > \tau_2$.

A significantly shorter interpolation time can be obtained using a Vernier scale, as shown in Fig. 8. [8].

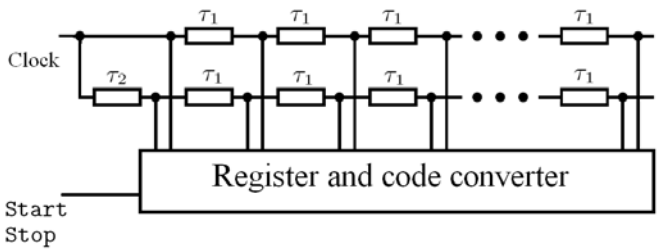


Fig. 8. Model of a Vernier multi-tapped delay line.

In this system the single-tap delay is equal to $\tau_1$ and the scale equation is given by:

$$\tau_2 = \left(p - \frac{1}{m}\right)\tau_1, \tag{3}$$

where: $p$ is the Vernier module and m is the Vernier dividing ratio.

The clock period is given by:

$$T = \frac{2N}{m}\tau_1, \tag{4}$$

where: $N$ is the width of the register.

Generally, the value of the Vernier module $p$ is an integer number. The number of taps and the single-tap delay strongly depend on the required system resolution. In this system the standard clock period should be very precisely adjusted to the single-tap delay. However it is a good method to increase the resolution of a TIMM, a very high influence of temperature fluctuation on DNL and INL is usually observed. INL can be limited to 140 ps and DNL to 80 ps using a Virtex XCV300 FPGA device in constant temperature [8].

The highest resolution of TIMM and a short interpolation-time can be obtained using a carry chain element as an element of a tapped delay line, as shown in Fig. 9. [8]. In such a way the TIMM resolution can be improved up to 50 ps, using Virtex 4 or Virtex 5 FPGA devices [8]. Moreover, maximal values of INL and DNL are limited to 50 ps and practically insensitive to temperature fluctuations. The double-pulse resolution in TIMMs presented above is usually limited to 5 ns.

If such resolution is not satisfied, then by simple replacement of the input signal start / stop and clock this parameter can be improved. A model of a multi-tapped delay line with replaced signals is shown in Fig. 10.

In such configuration, the double-pulse resolution is limited only by the bandwidth of FPGA circuits, but can be better than 3 ns. For effective memory space utilization, data from the delay-line register should be sent to the memory while at least one bit is different than zero.

It should be pointed out that the standard deviation of the measured time-interval strongly depends on standard clock quality [12]. The influence of accumulated jitter caused by phase

clock fluctuations on the time-interval-error (TIE) significantly increases while the time-interval range increases [12].

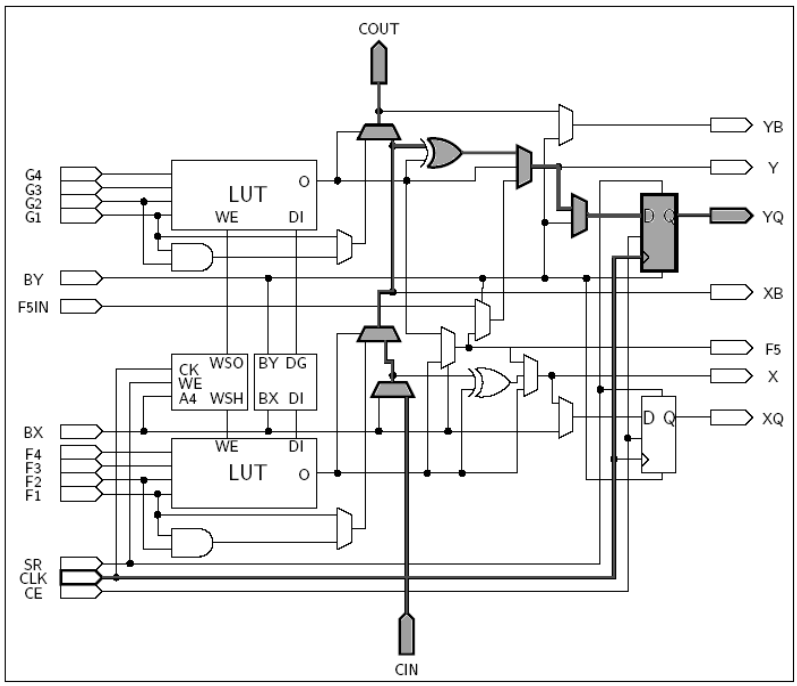


Fig. 9. Implementation of tapped delay line using carry chain elements.

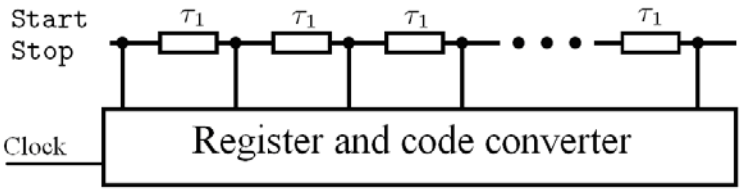


Fig. 10. Model of multi-tapped delay line with replaced signals.

## 5. Summary and conclusions

A single-stage TIMS implemented in a single FPGA can be a very flexible and effective virtual instrument, useful in many scientific and industrial applications. Relatively good parameters: DNL less than 50 ps, INL less than 50 ps, resolution better than 50 ps and double pulse resolution better than 3 ns can be achieved. Moreover, the design process of the TIMS does not have to be long or expensive. Metrological parameters of single-stage TIMS are now similar to multi-stage TIMS, while the architecture of the measurement modules is much simpler.

## References

[1] J. Kalisz: "Review of methods for time interval measurements with picosecond resolution". *Metrologia*, no. 41, 2004, pp. 17-32.

[2] W. Zhou, X. Ou, H. Zhou, B. Wang, X. Yang: "A Time Interval Measurement Technique Based on Time – Space Relationship Processing". *International Frequency Control Symposium and Exposition, IEEE*, June 2006, pp. 260-266.

[3] J. Song, Q. An, S. Liu: "A High-Resolution Time-to-Digital Converter Implemented in Field-Programmabl-Gate-Arrays". *IEEE Trans. On Nucl. Sci*., vol. 53, no. 1, Feb. 2006, pp. 236-241.

[4] R. Joost, R. Salomon: "BOUNCE, a Concept to Measure Picosecond Time Intervals with Standard Hardware". *Emerging Technologies and Factory Automation*, *ETFA 2008. IEEE International Conference*, Sept. 2008, pp. 1010-1015.

[5] Y. Liu, U. Vollenbruch, Y. Chen, C. Wicpalek, L. Maurer, Z. Boos, R. Weigel: "Multi-stage Pulse Shrinking Time-to-Digital Converter for Time Interval Measurements". *Wireless Technologies 2007 European Conference*, Oct. 2007, pp. 347-350.

[6] J. Jansson, A. Mäntyniemi, J. Kostamovaara: "A CMOS Time-to-Digital Converter With Better Than 10 ps Single-Shot Precision". *IEEE Jour. of Solid-State Circ*., vol. 41, no. 6, 2006, pp. 1286-1296.

[7] R. Szymanowski, J. Kalisz: "Field programmable gate array time counter with two-stage interpolation". *Review of Scientific Instruments*, vol. 76, no. 4, 2005, pp. 045104-045104-5.

[8] S. Grzelak: "Wysokorozdzielcze układy pomiaru odcinka czasowego dla zastosowań w spektrometrii fotonów i jonów". *Ph.D. Thesis*, Military University of Technology, Warsaw, 2006. (in Polish)

[9] D. Chaberski: "System pomiaru funkcji intensywności strumienia jonów w spektrometrii masowej czasu przelotu". *Ph.D. Thesis,* Military University of Technology, Warsaw, 2006. (in Polish)

[10] M. Zieliński, D. Chaberski, S. Grzelak: "Time-interval measuring modules with short deadtime". *Metrol. Meas. Syst.*, vol. X no. 3, 2003, pp. 241-251, 2003.

[11] M. Zieliński, D. Chaberski, M. Kowalski, R. Frankowski, S. Grzelak: "High-resolution time-interval measuring system implemented in single FPGA device". *Measurement*, vol. 35, no. 3, 2004, pp. 311-317.

[12] M. Zieliński, M. Kowalski, R. Frankowski, D. Chaberski, S. Grzelak, L. Wydźgowski: "Accumulated jitter measurement of standard clock oscillators". *Metrol. Meas. Syst.*, vol. XVI, no. 2, 2009, pp. 259-266.

[13] R. Frankowski, W. Wasilewski, M. Kowalski, M. Zieliński: "Wysokorozdzielczy dwukanałowy system Box-car implementowany w strukturze układu programowalnego Virtex4 dla zastosowań fizyki kwantowej". *Elektronika*, no. 5, 2008, pp. 21-23. (in Polish)

[14] Ł. Zaworski, S. Grzelak: "Układ pomiaru czasu dla przepływomierza ultradźwiękowego implementowany w strukturze FPGA". *Metrologia dziś i jutro*, Politechnika Gdańska, Gdańsk, 2009, pp. 281-288. (in Polish).

[15] M. Zieliński, A. Zawadzka, D. Chaberski: "Pomiary składu izotopowego wiązki atomowej z wykorzystaniem spektrometru masowego czasu przelotu". *Problemy metrologii elektronicznej i fotonicznej*, Politechnika Wrocławska, Wrocław, 2009, pp. 223-322. (in Polish)